



Form 1449 (Modified) Information Disclosure Statement By Applicant (Use Several Sheets if Necessary)	Atty Docket No. SNTCP001X2C1	Application No.: To Be Assigned
	Applicant: Lescot, et al.	Group To Be Assigned
	Filing Date July 12, 2001	

U.S. Patent Documents

Examiner Initial	No.	Patent No.	Date	Patentee	Class	Sub-class	Filing Date
<i>AG</i>	A1	5,238,860	08/24/93	Sawada, et al.			01/03/92
	A2	6,103,561	08/15/00	Seshadri, et al.			03/19/99

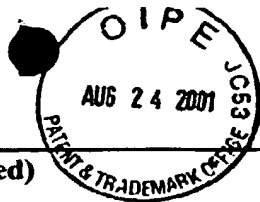
Foreign Patent or Published Foreign Patent Application

Examiner Initial	No.	Document No.	Publication Date	Country or Patent Office	Class	Sub-class	Translation	
							Yes	No
	A3							

Other Documents

Examiner Initial	No.	Author, Title, Date, Place (e.g. Journal) of Publication
<i>AG</i>	A4	Xavier Aragones, "A Contribution to the Study of Substrate Coupling in Mixed-Signal Integrated Circuits", Universitat Politecnica de Catalunya, October 1997
	A5	Francois Clement, "Computer Aided Analysis of Parasitic Substrate Coupling in Mixed Digital-Analog Cmos Integrated Circuits", Ecole Polytechnique Federale de Lausanne, 1996
	A6	Tallis Blalack, "Switching Noise in Mixed-Signal Integrated Circuits", Department of Electrical Engineering, Stanford University, December 1997
	A7	Tallis Blalack, Jack Lau, François J.R. Clément, and Bruce A. Wooley, "Experimental Results and Modeling of Noise Coupling in a Lightly Doped Substrate", 0-7803-3393-4, © 1996 IEEE, IEDM 96-623, pages 23.3.1 – 23.3.4.
	A8	Alan Pun et al., "Experimental Results and Simulation of Substrate Noise Coupling via Planar Spiral Inductor in RF ICs", Dept. of IEEE, The Hong Kong University of Science and Technology, Swiss Federal Institute of Technology and Hewlett-Packard Laboratory, 1997
<i>AG</i>	A9	Martin Pfost et al., "Modeling Substrate Effects in the Design of High-Speed Si-Bipolar IC's", IEEE Journal of Solid-State Circuits, Vol. 31, No. 10, October 1996
Examiner	<i>Rugh Jones</i>	
	Date Considered <i>6/24/04</i>	

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Examine r Initial	No.	Author, Title, Date, Place (e.g. Journal) of Publication
NA	B1	Sujoy Mitra et al., "A Methodology for Rapid Estimation of Substrate-Coupled Switching Noise", IEEE 1995 Custom Integrated Circuits Conference, 1995
	B2	Nishath K. Verghese et al., "Fast Parasitic Extraction for Substrate Coupling in Mixed-Signal ICs", IEEE 1995 Custom Integrated Circuits Conference, 1995
	B3	R. Gharpurey et al., "Modeling and Analysis of Substrate Coupling in Integrated Circuits", IEEE 1995 Custom Integrated Circuits Conference, 1995
	B4	Balsha R. Stanisic et al., "Addressing Substrate Coupling in Mixed-Mode IC's: Simulation and Power Distribution Synthesis, IEEE Journal of Solid-State Circuits, Vol. 29, No. 3, March 1994
	B5	Kuntal Joardar, "A Simple Approach to Modeling Cross-Talk in Integrated Circuits", IEEE Journal of Solid-State Circuits, Vol. 29, No. 10, October 1994
	B6	Thomas A. Johnson et al., "Chip Substrate Resistance Modeling Technique for Integrated Circuit Design", IEEE Transactions on Computer-Aided Design, Vol. CAD-3, No. 2, April 1984
	B7	T.A. Johnson et al., "Chip Substrate Resistance Modeling Technique for Integrated Circuit Design", IEEE, 1983
	B8	Ivan L. Wemple et al., "Mixed-Signal Switching Noise Analysis Using Voronoi-Tessellated Substrate Macromodels", 32 nd Design Automation Conference, 1995
	B9	R. Singh et al., "A Practical Approach to Modeling Substrate Coupling in Realistically-Large Mixed-Signal Designs", Department of Electrical and Electronic Engineering, University of Newcastle-upon-Tyne
	B10	Drago Strle, "Crosstalk in Mixed Signal Integrated Circuits: Problems and Solutions", University of Ljubjana
	B11	Talliss Blalack et al., "The Effects of Switching Noise on an Oversampling A/D Converter", 1995 IEEE International Solid-State Circuits Conference, 1995
	NA	B12
Examiner	Date Considered	
[Signature]		6/24/04

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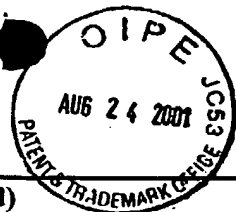


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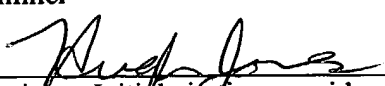
Examiner Initial	No.	Author, Title, Date, Place (e.g. Journal) of Publication
RJ	C1	Ranjit Gharpurey et al., "Modeling and Analysis of Substrate Coupling in Integrated Circuits", IEEE Journal of Solid-State Circuits, Vol. 31, No. 3, March 1996
	C2	Nishath K. Verghese et al., "Verification Techniques for Substrate Coupling and Their Application to Mixed-Signal IC Design", IEEE Journal of Solid-State Circuits, Vol. 31, No. 3, March 1996
	C3	T. Smedes et al., "Layout Extraction of 3D Models for Interconnect and Substrate Parasitics", ESSDERC'95 25 th European Solid State Device Research Conference, The Hague, September 1995
	C4	J.P. Raskin et al., "Coupling Effects in High-Resistivity Simox Substrates for VHF and Microwave Applications", Proceedings 1995 IEEE International SOI Conference, October 1995
	C5	R.B. Merrill et al., "Effect of Substrate Material on Crosstalk in Mixed Analog/Digital Integrated Circuits", IEEE, 1994
	C6	A. Viviani et al., "Extended Study of Crosstalk in SOI-SIMOX Substrates", IEEE Universite Catholique de Louvain, 1995
	C7	King H. Kwan et al., "Simulation and Analysis of Substrate Coupling in Realistically-Large Mixed-A/D Circuits", IEEE Symposium on VLSI circuits Digest of Technical Papers, 1996
	C8	Jean-Pierre Raskin et al., "Substrate Crosstalk Reduction Using SOI Technology", IEEE Transactions on Electron Devices, Vol. 44, No. 12, December 1997
	C9	Nishath K. Verghese et al., "Computer-Aided Design Considerations for Mixed-Signal Coupling in RF Integrated Circuits", IEEE Journal of Solid-State Circuits, Vol. 33, No. 3, March 1998
RJ	C10	Ranjit Gharpurey et al., "Transform Domain Techniques for Efficient Extraction of Substrate Parasitics", IEEE DSPSR&D Center, Texas Instruments Inc., 1997
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KD	D1	W. Liu et al., "R.F. MOSFET Modeling Accounting for Distributed Substrate and Channel Resistances with Emphasis on the BSIM3v3 SPICE Model", IEEE, 1997
	D2	Francois J.R. Clement, IC SUBSTRATE NOISE MODELING WITH IMPROVED SURFACE GRIDING TECHNIQUE, U.S. Patent Application No. 09/495,078, filed January 31, 2000, 57 pages.
KD	D3	Francois J.R. Clement, IC SUBSTRATE NOISE MODELING, U.S. Patent Application No. 09/262,735, filed March 4, 1999, 54 pages.
	D4	Jean-Michel Richer, IC SUBSTRATE NOISE MODELING INCLUDING EXTRACTED CAPACITANCE FOR IMPROVED ACCURACY, U.S. Patent Application No. 09/536,256, filed March 27, 2000, 89 pages.
Examiner 		Date Considered 6/24/04

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